EXHIBIT 4

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Optimum Design of Short-Channel 4H-SiC Power DMOSFETs

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Abstract. We describe an optimized design for the 1 kV short-channel 4H-SiC power DMOSFET, obtained from numerical simulations using the Taguchi method. Three new structural features are employed: (1) a current spreading layer (CSL) below the p-well, (2) a heavily-doped, narrow JFET region, and (3) a segmented p-well contact.

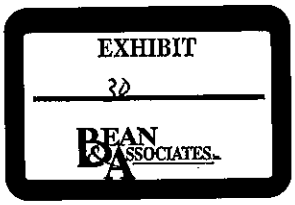
Introduction

This paper reports a detailed simulation study to optimize the performance of 4H-SiC vertical DMOS with a blocking voltage around 1 kV. Due to the low inversion channel mobility of 4H-SiC MOSFETs, the on-resistance of conventional SiC DMOSFETs at blocking voltages around 1 kV is mainly dominated by the channel resistance. To avoid this problem, a self-aligned short-channel technique has been developed and experimentally demonstrated [1]. This technique reduces the specific on-resistance $R_{on,sp}$ to below 10 mΩ-cm^2 in devices with a channel mobility of 25 cm^2/Vs. MEDICI™ simulations indicate that only about half of this resistance is contributed by the channel, with the other half attributable to the drift layer, JFET region, and source contact. Although an improved channel mobility will reduce the specific on-resistance, one quickly reaches the point where other components dominate, especially if a short channel ($\leq$ 0.5 μm) is employed. Since several resistance components other than channel resistance are significant in the short-channel device, a global optimization is performed to achieve minimum specific on-resistance at a given blocking voltage. To further improve the performance, we introduce three new features: (1) a heavily-doped current spreading layer (CSL) under the p-base to reduce current crowding at the corner of p-base, (2) a heavily-doped, narrow JFET region, (both the highly doped layers are formed by separate epilayers), that minimizes cell area, and (3) a segmented p-well contact that minimizes the overall source resistance and the cell area.

Optimization Methodology

A cross section of the simulated device is shown in Fig. 1. Note the introduction of an n-type current spreading epilayer (CSL) immediately below the p-well. The blocking voltage V_B of the device is defined as the drain voltage at which either: (i) avalanche breakdown occurs, or (ii) the gate oxide field exceeds 4 MV/cm. Introduction of the CSL and a heavily-doped JFET region tend to increase the oxide field in the blocking state, due to the higher doping. The use of a narrow JFET region helps screen the oxide field and reduces cell area, but increases JFET resistance.

Since a number of parameters influence the performance of the device, the Taguchi method [2] is used to investigate the relative influence of each parameter. For example, varying JFET width between 1 – 4 μm has a 54% effect on blocking voltage, but only a 14% effect on specific on-resistance. This difference in sensitivity allows us to increase V_B without significantly increasing



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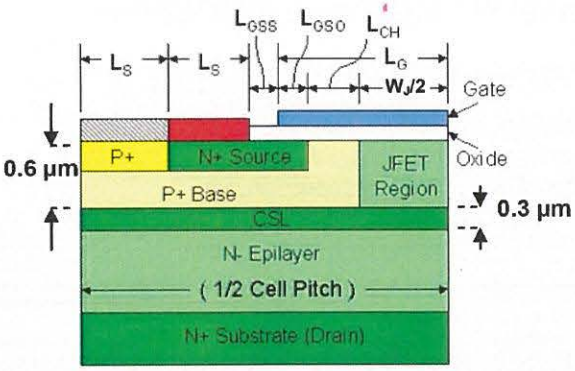

Figure 1. Cross section of the structure simulated, with critical dimensions identified. L_{CH} = 0.5 µm.

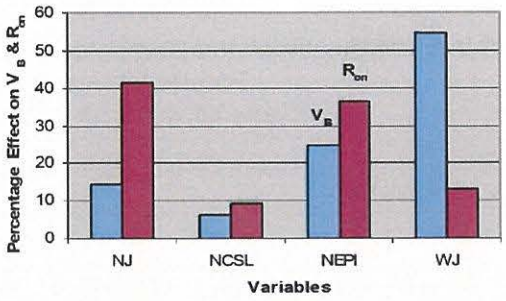

Figure 2. Percentage effect of different design parameters, as indicated by the Taguchi method.

$R_{on,sp}$. Figure 2 compares the relative sensitivity of V_B and $R_{on,sp}$ to variations in JFET doping (N_J), CSL doping (N_{CSL}), epilayer doping (N_{EPI}), and JFET width (W_J). Blocking voltage is most strongly affected by JFET width, but is relatively insensitive to JFET and CSL doping. On-resistance is most strongly influenced by JFET and epilayer doping, but is insensitive to CSL doping and JFET width.

Variation of Device Performance with Design Parameters

Figure 3 shows the variation of V_B and $R_{on,sp}$ with JFET width W_J. The blocking voltage is oxide-limited except for W_J = 0.5 µm and 1 µm. As shown in Fig. 3, V_B is a strong function of JFET width, whereas $R_{on,sp}$ is relatively insensitive unless W_J is reduced below 1 µm. These competing effects produce a sharp peak for V_B^2/R_{on} at a JFET width around 1µm.

A similar analysis is performed for epilayer doping, CSL doping, and JFET doping, and the results are shown in Figs. 4 – 6 respectively. In each of these figures, JFET width is held at 1 µm. Increasing the doping of any of these layers reduces the on-resistance, but has a negative effect on the blocking voltage. The values quoted for blocking voltage, over the entire range of epilayer and CSL doping, are avalanche breakdown voltage, since a JFET width of 1 µm effectively screens the gate oxide from the electric field, keeping the oxide field below 4 MV/cm. As shown in Fig. 7, a

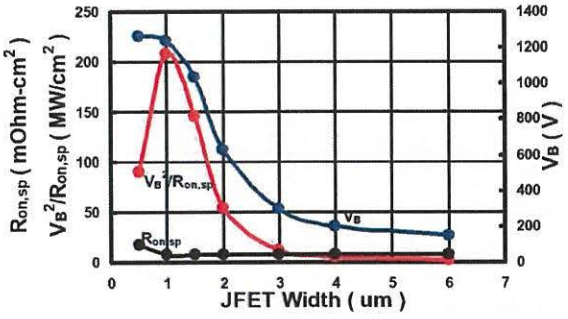

Figure 3. Effect of JFET width on V_B, $R_{on,sp}$, and $V_B^2/R_{on,sp}$. N_{EPI} = 1x10^{16} cm^{-3}, N_{CSL} =1x10^{17} cm^{-3}, N_J = 5x10^{16} cm^{-3}, L_{CH}= 0.5 µm.

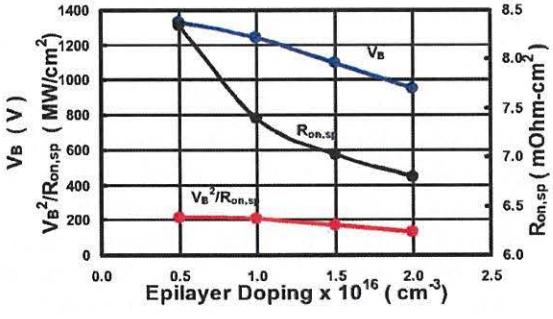

Figure 4. Effect of epilayer doping on V_B, $R_{on,sp}$, and $V_B^2/R_{on,sp}$. W_J = 1 µm, N_{CSL} =1x10^{17} cm^{-3}, N_J = 5x10^{16} cm^{-3}, L_{CH}= 0.5 µm.

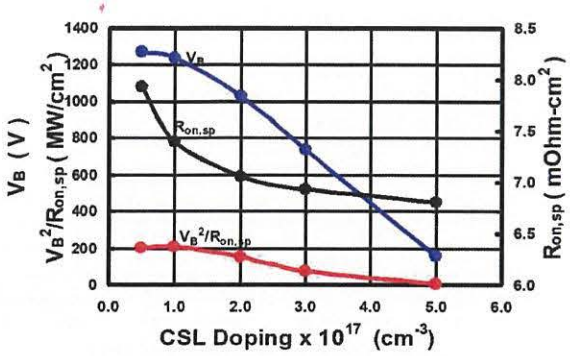

Figure 5. Effect of CSL doping on V_B, $R_{on,sp}$, and $V_B^2/R_{on,sp}$. W_J = 1 μm, N_{EPI} =1x10^{16} cm^{-3}, N_J = 5x10^{16} cm^{-3}, L_{CH}= 0.5 μm.

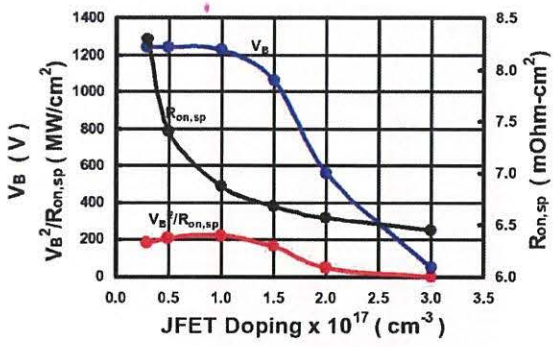

Figure 6. Effect of JFET region doping on V_B, $R_{on,sp}$, and $V_B^2/R_{on,sp}$. W_J = 1 μm, N_{EPI} =1x10^{16} cm^{-3}, N_{CSL}= 1x10^{17} cm^{-3}, L_{CH}= 0.5 μm.

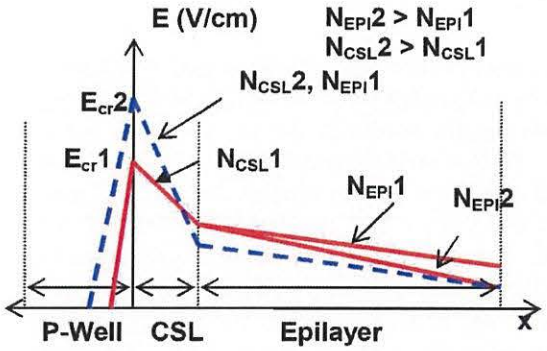

Figure 7. Electric field profiles for different epilayer and CSL dopings.

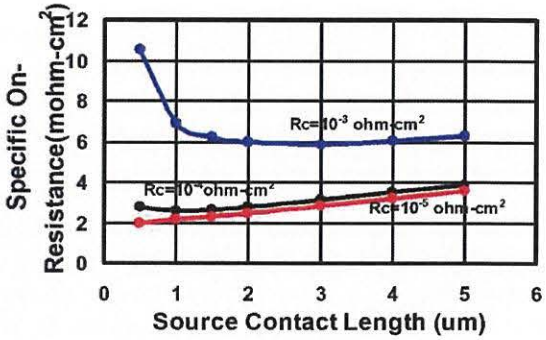

Figure 8. $R_{on,sp}$ as a function of source contact length for several values of source contact resistivity R_C.

higher CSL doping increases the critical electric field at the junction of CSL and p-base, but also increases the slope of the electric field within the CSL, so the avalanche breakdown voltage falls sharply with CSL doping. On the other hand, increasing the JFET doping increases the oxide field sharply, and reduces the oxide-limited blocking voltage. It is worth noting that even a JFET width of 1 μm is not able to protect the gate oxide for JFET dopings higher than 1.5x10^{17} cm^{-3}.

Taking into account the effect of each of these parameters, we find that the maximum $V_B^2/R_{on,sp}$ can be achieved for a JFET width of 1 μm, epilayer doping of 1x10^{16} cm^{-3}, and CSL and JFET doping of 1x10^{17} cm^{-3}. This optimum design results in a blocking voltage of **1,230 V** (limited by avalanche breakdown, with an oxide field of 3.56 MV/cm at breakdown), a specific on-resistance of **6.88 mΩ-cm^2**, and a $V_B^2/R_{on,sp}$ of **220 MW/cm^2**, assuming a modest channel mobility of 25 cm^2/Vs. This design provides an improvement of around 150% in the oxide-limited blocking voltage, even though the reduction in the specific on-resistance is only 20%.

Since we are approaching the theoretical limit for SiC, it is difficult to reduce the total on-resistance further, but a reduction in cell pitch helps reduce $R_{on,sp}$. Conventional optical lithographic

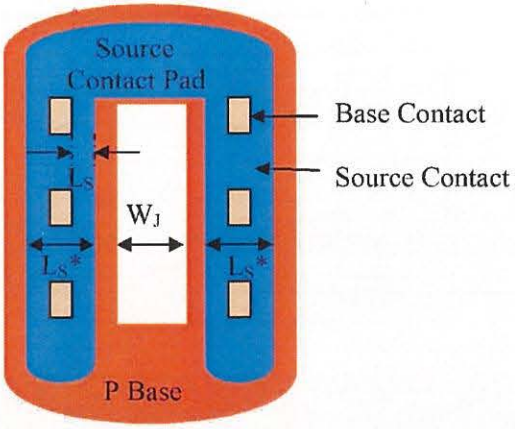

Figure 9. Layout of a DMOSFET with discontinuous (segmented) p-base contacts.

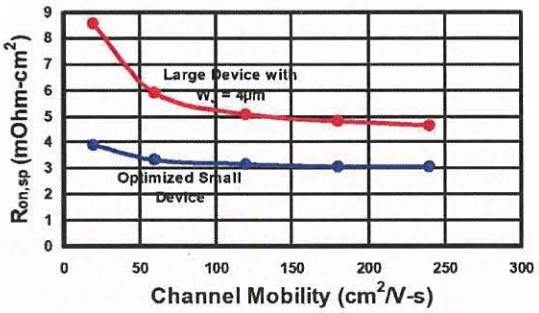

Figure 10. Effect of channel mobility on the specific on-resistance of the conventional and optimized device.

techniques can produce gate source overlaps (L_{GSO}) and gate source separations (L_{GSS}) $\leq$ 0.5 µm. On the other hand, the source contact length is found to have a strong effect on $R_{on,sp}$, and selecting a source contact length slightly greater than the transfer length produces the lowest $R_{on,sp}$ for a specific value of contact resistivity, as shown in Fig. 8. With a contact resistivity $R_C = 5x10^{-4}$ Ω-cm^2, the optimized device exhibits an $R_{on,sp}$ of 4.23 mΩ-cm^2 for a source contact length of 2 µm, and with $R_c = 1x10^{-5}$ Ω-cm^2, $R_{on,sp}$ can be reduced to 2.0 mΩ-cm^2, which represents almost a factor of five improvement over the previously obtained result. A segmented pbase contact, as shown in Fig. 9, helps to obtain wider source contact without affecting the cell pitch and thereby helps to reduce $R_{on,sp}$ It is interesting that the channel mobility is not at all significant for this optimized device, as shown in Fig. 10. In other words, increasing the channel mobility above about 50 cm^2/Vs produces very little improvement in performance for this aggressively scaled device.

Summary and Conclusions

A global optimization has been performed to maximize the figure-of-merit $V_B^2/R_{on,sp}$ of 1 kV self-aligned short-channel power DMOSFETs in 4H-SiC. Three novel features are included in the design: (1) a heavily-doped n-type current spreading layer under the p-base, (2) a heavily-doped, narrow JFET region, and (3) a segmented p-well contact. The fully optimized device can achieve a specific on-resistance as low as 2.0 mΩ cm^2 at a blocking voltage of 1 kV, assuming a channel mobility of 25 cm^2/Vs. This is a factor of five lower than the short-channel device reported by us earlier [1].

Acknowledgements

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References

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